



# FASTER REGULATORY COMPLIANCE WITH VIRTUAL EMC TESTING

Early-stage virtual testing helps meet EMC standards

## INDUSTRY CHALLENGES

Designing a device, equipment or other electrical system to meet Electromagnetic Compatibility (EMC) requirements and regulations is challenging and carries high stakes for a vendor. There is a wide range of mandatory global and regional standards. Without certification, a product cannot be sold.

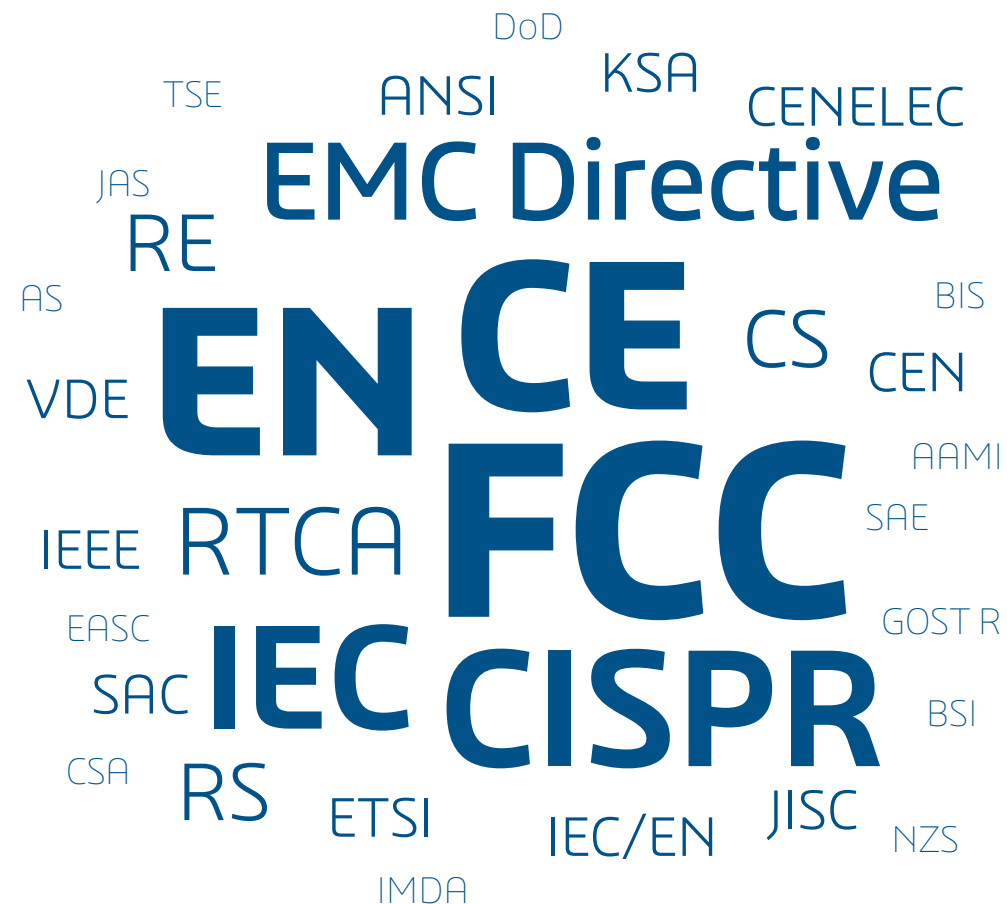
A modern electronic system can generate external interference through several mechanisms and can be susceptible to outside interference affecting its operation. As a result, EMC design is a necessary but often lengthy and time-consuming process. Traditionally, EMC effectiveness is assessed late in the development cycle once a physical prototype is available for testing in a specialist facility.

If a device or system fails during testing, the entire development process can be derailed and the cost of reworking the product may be considerable. Even worse, problems that emerge after a product has gone on sale can result in expensive recalls, warranty claims and, potentially, reputational damage and legal liability.

**Successful early-stage design for EMC compliance is a major factor in ensuring a product is brought to market quickly without risk of failure at either the testing or sales stages.**

In this e-book, we examine how component developers and system integrators can use virtual testing in a software environment early in the development cycle to help ensure that devices meet EMC requirements and regulations.

Electromagnetic Compatibility (EMC) ensures that electronic devices and systems function properly in their electromagnetic environment without causing or experiencing interference. EMC is essential to the safe, reliable operation of electronics, and devices must meet EMC regulations to be sold.



## MARKET SITUATION

- **Continued growth:** The number of IoT or connected objects worldwide is forecast to almost double to more than 32.1 billion devices in 2030<sup>1</sup>.
- **Rising complexity of electronic systems:** Modern electronic systems with multiple wireless systems and numerous variants, require more complex EMC compliance measures.
- **Sensitive electronics:** PCBs, ICs and other electronic components are susceptible to damage from electrostatic discharge (ESD).
- **High-speed electronics:** Modern connected devices operate at higher data rates and frequencies than prior generations of electronics, potentially leading to higher levels of radiated emissions. There's a trend toward lower voltage levels to reduce power consumption, which makes electronic devices more susceptible to external fields.
- **Rapidly evolving standards:** Every electronic device has to achieve EMC certification. Each geographical region has its own set of regulatory compliance standards. Keeping up with varying and evolving EMC regulations can be challenging, requiring continuous updates to compliance processes.
- **Non-compliance** can have serious consequences, including fines, product recalls and removal from sale.



<sup>1</sup> <https://www.statista.com/statistics/1183457/iot-connected-devices-worldwide/>



## VIRTUAL TWIN EMC TESTING

EMC testing is typically carried out in the lab or specialist facility with various scenarios created according to the standards. Performing these tests requires physical prototypes and for certain destructive tests, such as ESD, potentially a large number of prototypes. Significant time and costs such as labor, equipment and facility access are associated with physical testing. Replacing some of these with **virtual tests can bring significant efficiency gains**.

Simulation enables EMC tests to be performed on a **virtual twin** (see box) of the device. Standard tests can be replicated reliably in the virtual environment. Test equipment such as EMC antennas, ESD generators and anechoic or reverb chambers can be included either as a full 3D representation or as an equivalent, and often faster, fully virtual test.

A virtual twin simulation can deliver results and KPIs in line with a physical test, including current, voltage and field strength at any point in the test set-up at all frequencies and times. It can even **calculate data that is impossible to test physically** and visualize this in 3D. By exploring the 3D visualization, engineers can trace the propagation of fields and currents and identify coupling paths and the root causes of issues.

### What is a virtual twin?

A model is only helpful if its behavior matches that of the real-world system it represents. A virtual twin combines all the available data about a system into a single model to produce as accurate a representation as possible of the system. A validated virtual twin gives users confidence that the simulation results correspond to actual behavior.



2 [https://commons.wikimedia.org/wiki/File:Reverberation\\_chamber.jpg](https://commons.wikimedia.org/wiki/File:Reverberation_chamber.jpg)

Manuamador, CC BY-SA 3.0 <<https://creativecommons.org/licenses/by-sa/3.0/>>, via Wikimedia Commons

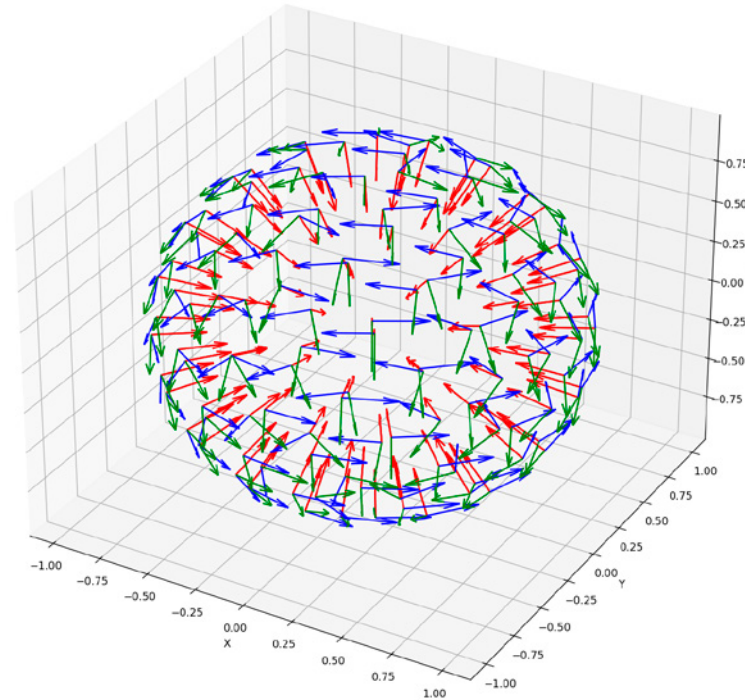
## VIRTUAL TWIN EMC TESTING

EMC testing and compliance work has traditionally been conducted in hardware by experienced EMC engineers. Over recent years, engineers have started to see the benefits and reliability of simulation, particularly in the earlier stages of the design process. Hardware and chamber testing can be reserved for the later stages of the process. It is widely accepted that real and virtual tests are complementary and both are essential to bring products to market as quickly as possible.

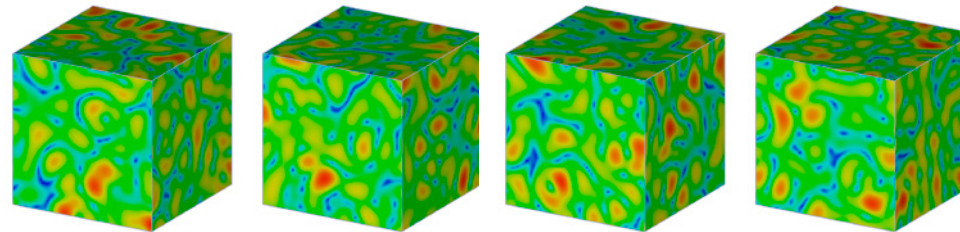
When you test a complete hardware prototype, the nature of that test means that all the real-world effects are included and as a result, you get an overall pass or fail result. Great if it passes, but with a failure, it can be difficult to get to the root cause, due to a lack of additional information. Rework or patching is the typical response, but there is no guarantee of success in subsequent tests.

On the other hand, the virtual twin simulation gives you detailed information about field and current behavior, which can help to pinpoint the cause of problems. Changes can then be made in the virtual model and retested rapidly.

### Virtual reverberation chamber simulation



A one-meter-radius sphere where each of the red arrows represents a plane wave propagating towards the center of the sphere where the device under test (DUT) is located. The blue and green arrows show two orthogonal polarizations of the plane waves.



The generated field sources which are used to drive the simulation. Four sets of randomized plane waves are combined to achieve the statistical uniformity required by the susceptibility standard.

# VIRTUAL TWIN EMC DESIGN PROCESS

## TRADITIONAL EMC DESIGN

*(Weeks to months)*

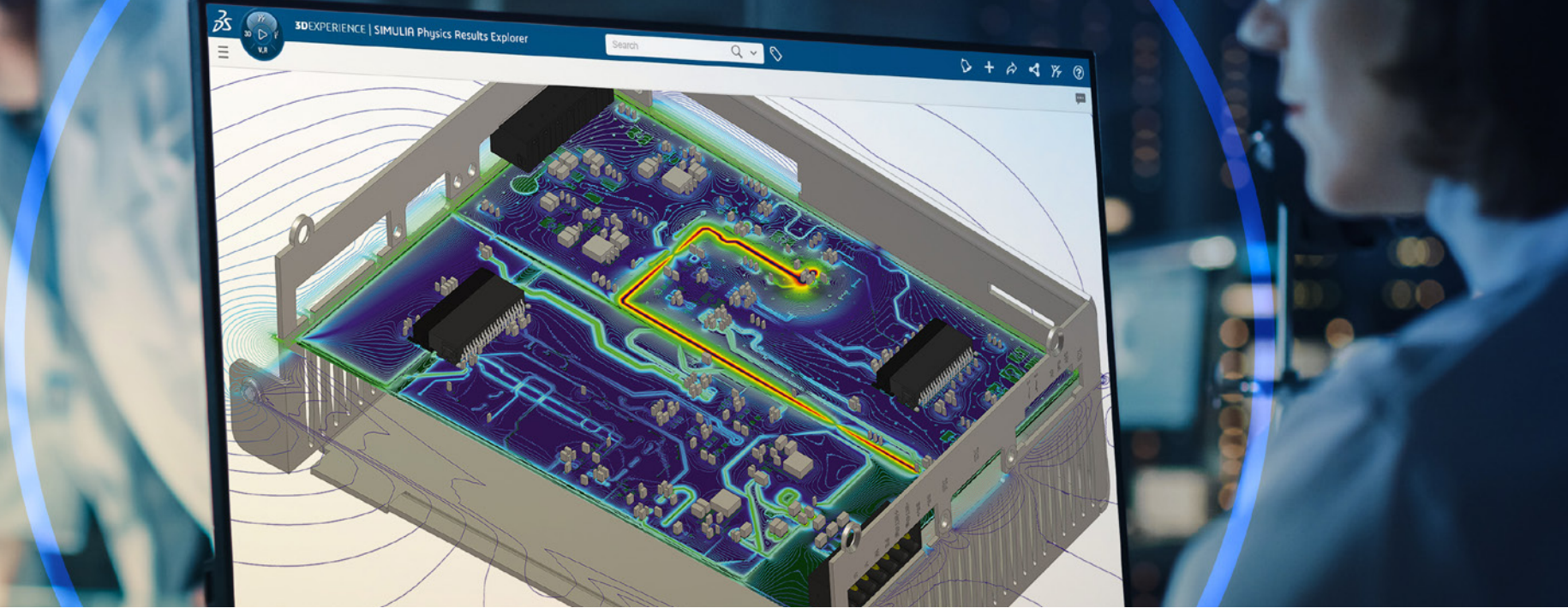


*The virtual twin EMC design process significantly reduces the time and costs for certification and market entry.*

## VIRTUAL TWIN EMC DESIGN

*(Days)*





## BENEFITS OF EMC SIMULATION

### Accelerate development

- Explore numerous design configurations quickly, identifying potential issues early in the design process
- Reduce the need for multiple physical prototypes and iterations
- Faster product to market

### Validation and certification

- Ensure the performance of installed supplied parts and the complete system
- Exploration of full design space before building physical prototype
- Achieve optimum trade-offs between performance, compliance & industrial design

### Reduce costs

- Reduce reliance on physical tests
- Reduce number of physical prototypes
- Achieve regulatory compliance via simulation as allowed<sup>3</sup>
- Full traceability throughout process to ensure designers and engineers are in sync

### Enhance quality

- Evaluate device-level emissions
- Optimize products for improved performance and reliability
- Ensure reliable communication while meeting emissions regulations
- Ensure susceptibility goals are met

<sup>3</sup> <https://blog.3ds.com/brands/simulia/simulation-5g-smartphone-fcc-certification/>

## SIMULATION FOR EMC COMPLIANT DESIGN

EMC encompasses various phenomena. EMC regulations typically specify that a device must not cause interference to other devices (emissions) and must be able to withstand interference from other devices (susceptibility). Interference can manifest as conducted currents, such as through wires and cables, or as radiated fields, for example, from antennas or unintentional resonances. It can occur between components of a single system (such as desense or co-site interference) or between multiple devices, including artificial devices and natural phenomena such as electrostatic discharge (ESD).

In this section, we explain how simulation can be used to analyze EMC from many perspectives.

- Emissions (conducted & radiated)
- Susceptibility
- Electrostatic discharge
- System integration
- EMC rule-checking





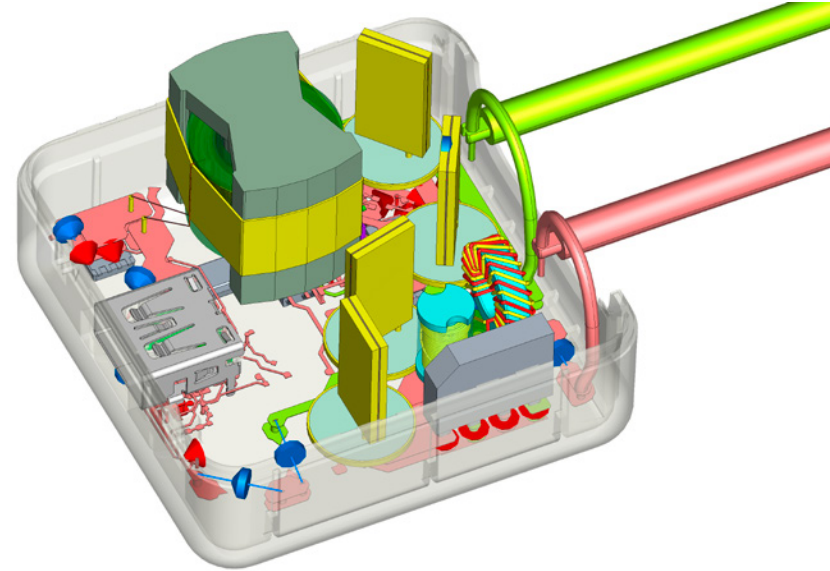
## EMISSIONS

EMC regulations cover interference from emissions of all kinds from devices—both intended and unintended. Antennas emitting outside the allowed frequency band or at too high a power level, components and signal lines resonating like antennas, and spurious currents on cables to other devices: these can all cause interference with other devices or exceed limits for human body absorption.

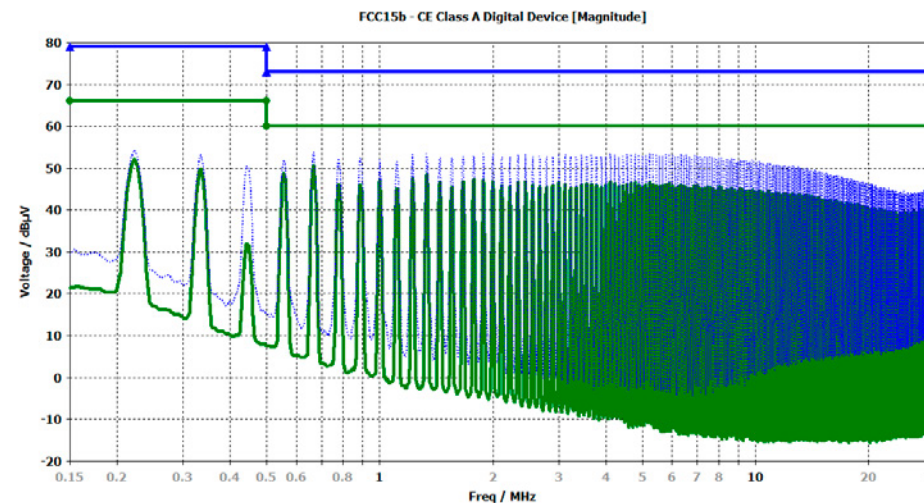
### CONDUCTED EMISSIONS

Many electronic devices require power conversion, which can be AC-DC, DC-AC, or DC-DC. During the conversion process, high-frequency noise can be observed at the input power supply, leading to conducted emissions.

Seamless integration between the 3D full-wave solver and circuit simulation enables users to simulate conducted emissions efficiently. Useful post-processing tools, such as surface current visualization from the system response, help identify the current distribution. A current probe records the common mode current, and a virtual EMI receiver can deliver results similar to measurement equipment.



Model provided by Dassault Systèmes customer.

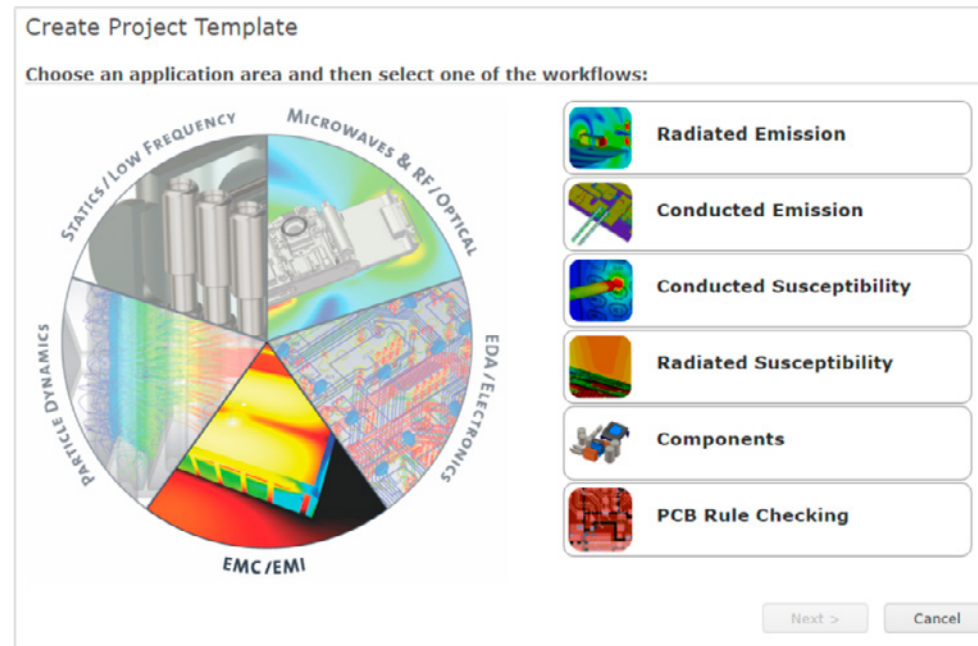


Power inverter. Virtual pre-compliance workflow simulates conducted emissions according to the FCC Part 15B standard. The blue curve is the Quasi-Peak (QP) and the green curve is the average (AVG).

## RADIATED EMISSIONS

Radiated emissions can be tested in the laboratory with receiver antennas positioned around the DUT in all directions. This set-up can be quickly and automatically replicated on a virtual twin of the device in the simulation environment. **Virtual probes can measure fields at any point inside or outside the DUT to give a comprehensive understanding of the device's emissions.**

Even very small details—for example, an individual signal trace on a PCB or a seam in the casing—can lead to radiated emissions. Solver methods such as transmission line matrix (TLM) are well-suited to the simulation of these kinds of problems due to their ability to use mesh-lumping and compact models to represent EMC-relevant features efficiently and accurately.



EMC project set-up is accelerated with templates for a wide range of test scenarios

An EMC Wizard can automatically set up simulations according to common EMC standards. Virtual test equipment, such as test antennas, ESD guns, and bulk current injection (BCI), is available in a library of components for direct import into any project. EMC post-processing converts simulation results into common EMC KPIs.





## SUSCEPTIBILITY

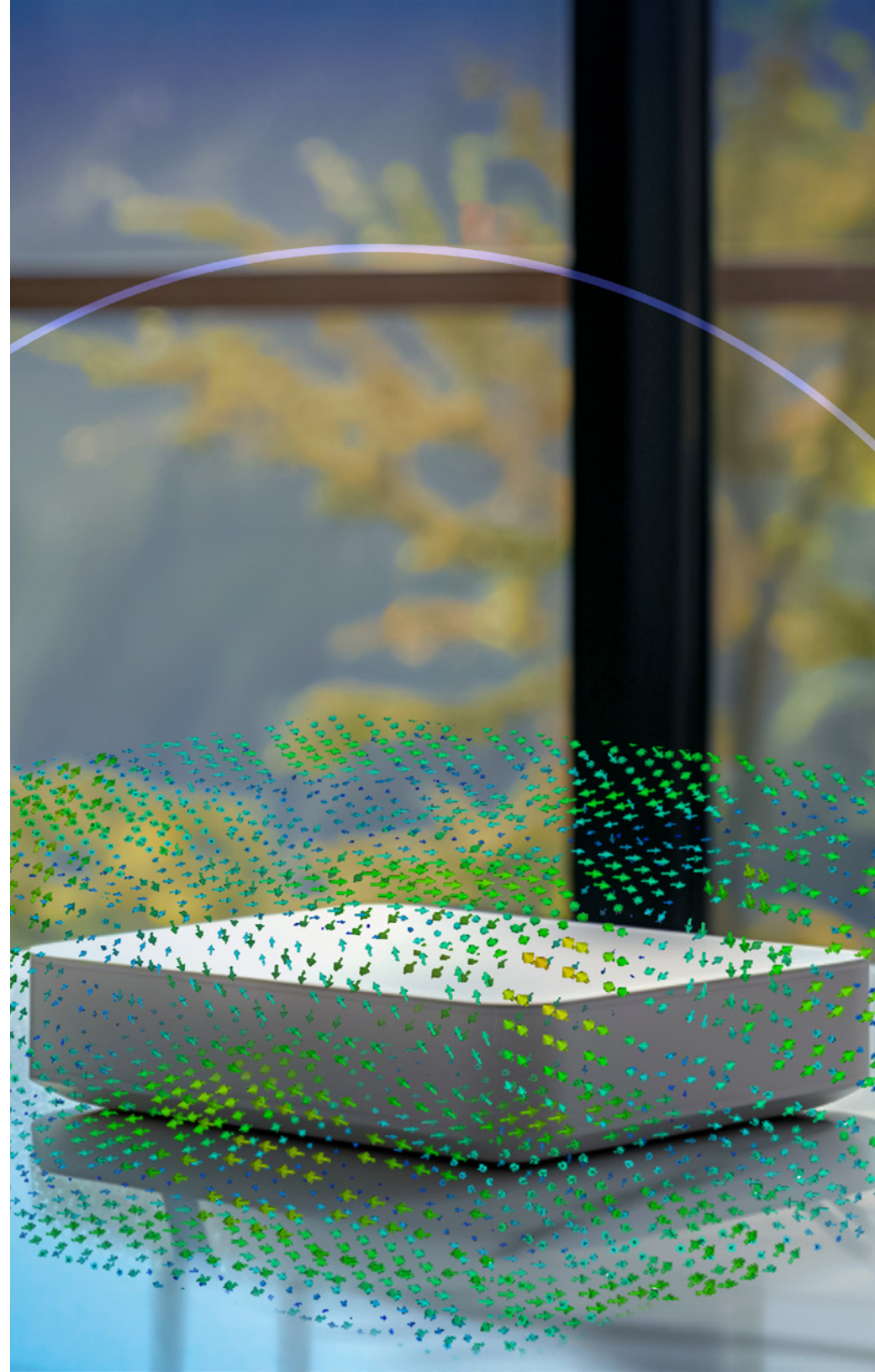
Devices can create emissions higher than certified levels through either actual antennas or unintended resonances in components acting as antennas. Similarly, devices can be susceptible to external signals by the same mechanisms. Although not regulated, it's very important for device reliability and OEM warranty issues to ensure that the device is well protected from external interference sources.

The typical test procedure uses a reverberation (reverberation) chamber. A reverberation chamber is a screened, metal-walled room; in technical terms, a cavity resonator with a high Q factor. This means that low input power can generate the high field strengths required for the tests. However, the distribution of the fields is uneven due to the standing waves created and a DUT might not receive the desired field levels. To fix this problem, mechanical rotating "mode stirrers"<sup>4</sup> are used to rotate the fields to ensure the DUT receives the required field levels.

Reverberation chambers are expensive to locate, hire and operate. **Virtual test offers a new and reliable approach that replicates the test procedure using a set of spherically distributed field sources with random polarizations—delivering a statistically uniform field to the DUT.**

Virtual router test, showing field source designed to replicate real-world reverberation chamber tests.

<sup>4</sup> <https://absolute-emc.com/product/reverb-chamber>



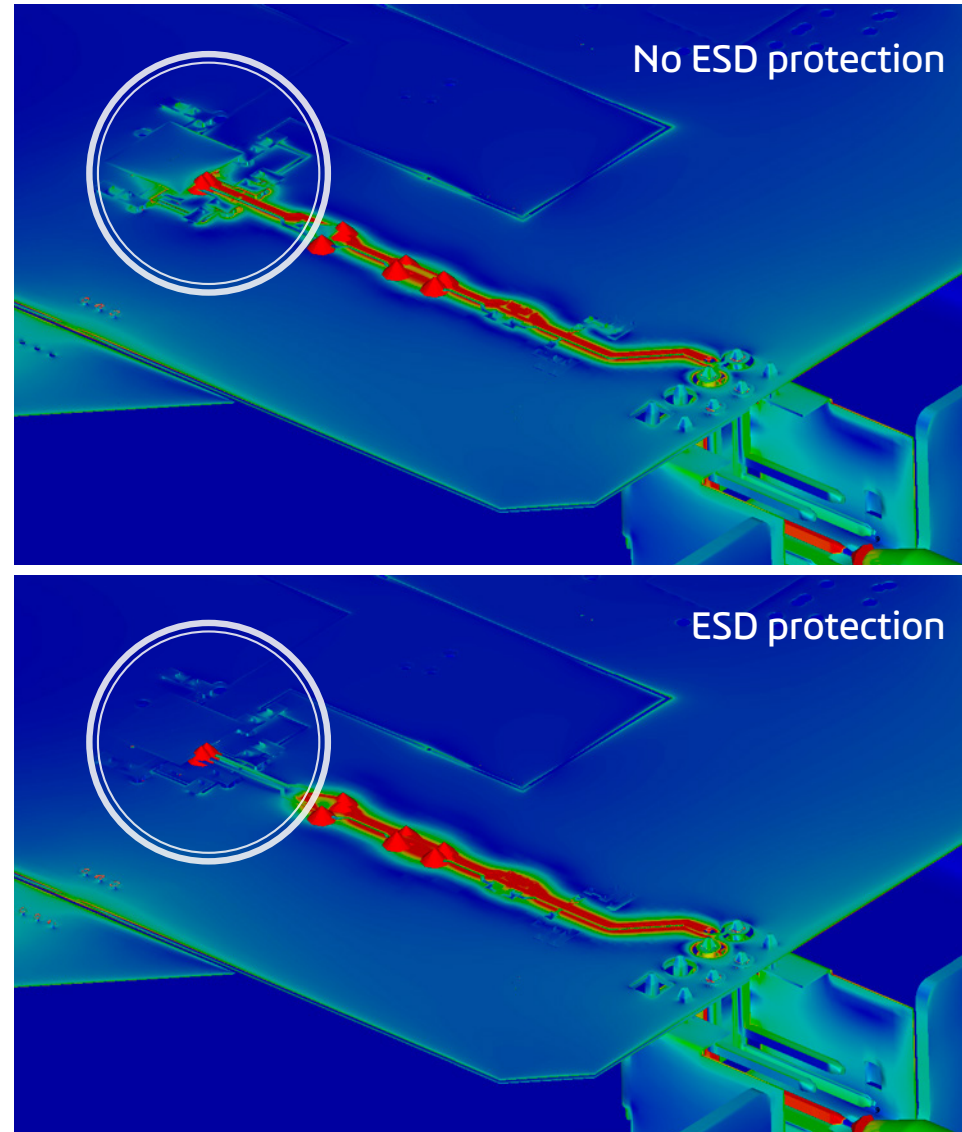
## ELECTROSTATIC DISCHARGE

Electrostatic discharge (ESD) occurs when a static electric charge discharges to earth through the device. ESD can lead to spurious signals and data errors and even damage or destroy components entirely.

Testing in the ESD laboratory is time-consuming and expensive, particularly if multiple prototypes are damaged. If problems are revealed during testing, resolving them can delay development and increase costs.

Simulation can replicate ESD tests virtually. Both the test equipment and the device under test (DUT) are created virtually. Any scenario, including both contact and air-gap ESD, can be modeled, taking into account the breakdown of air.

**With simulation, electrostatic discharge can be analyzed faster and more cost-effectively than by physical testing.**



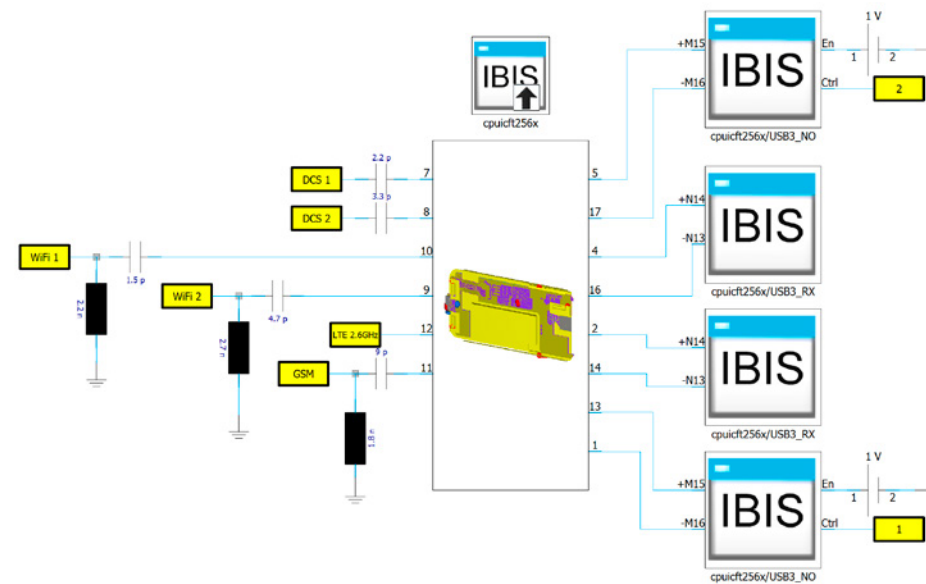
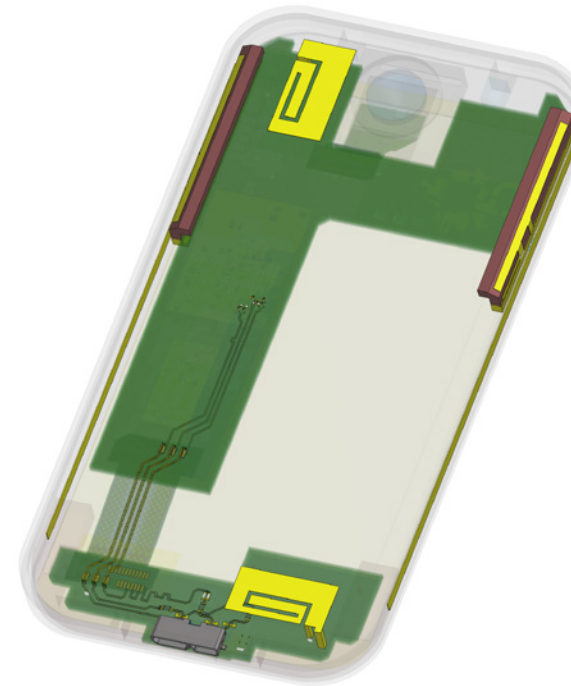
Simulated surface currents on an ethernet system without ESD protection (top), and with protection (bottom). Simulation demonstrates that the diode protects the sensitive chips from the incoming currents.



## SYSTEM INTEGRATION

Ensuring EMC compliance in individual components is not enough. When integrating multiple components into a system, their interactions can lead to unforeseen EMC issues. For example, a spurious frequency from one component can be conducted to another component that radiates it. System-level simulation of all components together is necessary to identify and resolve these kinds of issues.

- Challenge of system integration in limited space
- Evaluation of RF interference between high-speed signals and antennas through simulation
- Early prediction and measures to prevent RF interference



3D EM field and circuit co-simulation of RF interference between mobile phone antennas and high-speed USB interface.

## EMC RULE CHECKING

Electronic engineers must follow many design rules during PCB design and system integration to reduce the risk of EMC and signal integrity and power integrity (SI/PI) problems, such as maintaining spacing between components or avoiding long signal traces. However, with dozens of rules to check on densely populated multi-layer PCBs, potential problems can easily be missed. Preventing EMC problems at the design stage is more time-efficient than attempting to fix them late in development.

Automatic EMC rule checking identifies violations of design rules even at the very beginning of layout. Where issues are identified, the software gives information about the nature of the rule violation, helping engineers to re-design the board to remove the EMC risk. **Automatic rule-checking supplements simulation: the rule checker provides a rapid overview of potential issues, and once these are resolved, full-wave simulation can identify any issues caused by complex 3D interactions outside the scope of the design rules.**



Index	Net Name	Layer	Type of Violation	Outside Layer Segment(s)
0	DAT3	LR4	Chain Seg(s)	LR4
1	DAT4	LR4	Chain Seg(s)	LR4

Rule-checking automatically highlights potential EMC issues, such as a long, exposed trace shown here.





## UNIFY MODELING AND SIMULATION WITH MODSIM

In a highly competitive market, manufacturers must ensure that their processes are up to the job, as innovation and being first to market are crucial for a product's success. Rethinking processes to ensure product designers collaborate with simulation engineers on a common data model enables better communication and faster feedback loops. Shifting simulation to the earliest stage of the product design process enables shortened development and certification processes, resulting in faster product delivery.

We call this the unified modeling and simulation process—MODSIM for short.

- **Simplified process with a single source of truth:** Teams can collaborate efficiently on a single platform during development until the start of production (SOP).
- **Faster design iterations:** The same data is used for all design and analysis tasks, saving time and development costs and reducing project complexity.
- **Design in any tool:** Flexibility to choose your preferred design tools: CATIA and SOLIDWORKS from Dassault Systèmes or third-party CAD and ECAD tools.

## WHY SIMULATE

The modeling and simulation technology from Dassault Systèmes helps engineering teams to design, understand, optimize and validate their devices and equipment at an early stage of the product development cycle. Virtual twins give high confidence that a device will pass regulatory compliance certification and meet required KPIs before physical testing begins.



### First to Market

Avoid late entry to market. Obtain design feedback, identify issues and resolve them rapidly.



### Innovation

Test the viability of innovations early in development. Use DOE to explore the design space to find potential solutions.



### Regulatory Compliance

Simulation can significantly accelerate regulatory compliance certification, reduce the risk of failure and increase confidence that the final design passes first time.



### Optimize Products

Simulation enables optimization to reduce weight, cost and energy consumption while improving space usage and performance.



### Virtual Testing

Virtual twins let you visualize and simulate multiple real-world test-cases and can model years of use in just hours.



### Cost Savings

Accelerate product development cost-effectively using virtual twins. Avoid the risk of expensive late-stage design changes.

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